Application Considerations and Circuits for a New Chopper-Stabilized Op Amp

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A great deal of progress has been made in op amp DC characteristics. Carefully executed designs currently available provide sub-microvolt V_{OS} ΔT drift, low bias currents and open loop gains exceeding one million. Considerable design and processing advances were required to achieve these specifications. Because of this, it is interesting to note that amplifiers with even better DC specification were available in 1963 (Philbrick Researches Model SP656). Although these modular amplifiers were large and expensive ($\approx 3'' \times 2'' \times 1.5''$ at $195.00 1963 dollars) by modern standards, their DC performance anticipated today's best monolithic amplifiers while using relatively primitive components. This was accomplished by employing chopper-stabilization techniques (see Box, "Choppers, Chopper-Stabilization and the LTC1052") instead of the more common DC-differential stage approach.

The chopper-stabilized approach, developed by E. A. Goldberg in 1948, uses the amplifier's input to amplitude modulate an AC carrier. This carrier, amplified and synchronously demodulated back to DC, furnishes the amplifier's output. Because the DC input is translated to and amplified as an AC signal, the amplifier's DC terms have no effect on overall drift. This is the reason chopper-stabilized amplifiers are able to achieve significantly lower time and temperature drifts than classic differential types. Additionally, the AC processing of the signal aids low frequency amplifier noise performance and eliminates many of the careful design and layout procedures necessary in a classic differential approach. The most significant trade-off is increased complexity. The chopping circuitry and sampled data operation of these amplifiers require significant attention for good results. Additionally, the AC dynamics of chopper-stabilized amplifiers are complex if bandwidths greater than the chopping carrier frequency are required.

The LTC1052 is a third generation monolithic chopper-stabilized amplifier. As the table in Figure 1 shows, it is significantly better than previous monolithic chopper-stabilized amplifiers in several areas. For comparison purposes, conventional FET input and bias current compensated bipolar types are also listed. Noise has been a

PARAMETER	LTC1052 CHOPPER-STABILIZED	ICL7652 CHOPPER-STABILIZED	HA2904/5 CHOPPER-STABILIZED	AD547 FET	LM11 LOW I_B BIPOLAR	LT1012 LOW I_B BIPOLAR
E_{OS} – 25°C	±5μV	±5μV	±50μV	±250μV	±300μV	±35μV
E_{OS} ΔT/°C	0.05μV/°C	0.05μV/°C	0.4μV/°C	1μV/°C	3μV/°C	1.5μV/°C
Noise (1Hz BW)	0.5μVp-p Typ	0.2μVp-p Typ*	Specified as 900nV/√Hz at 10Hz**	4μVp-p	6μVp-p $R_S = 100k\Omega$	0.5μVp-p
Open Loop Gain	120dB	120dB (25°C)	5×10^8 Typ	2.5×10^5	2.5×10^5	3×10^5
Bias Current—25°C	30pA	30pA	150pA Typ	25pA	50pA	100pA
CMRR	120dB	110dB (25°C)	120dB	80dB	110dB	114dB
PSRR	120dB	110dB (25°C)	120dB	100dB	100dB	114dB
Input Common-Mode Range	$V^+/-2.3V$ $V^-/+0V$	$V^+/-1.5V$ $V^-/+0.7V$	±10V at ±15V Supply	$V^+/-2V$ $V^-/+3V$	$V^+/-0.5V$ $V^-/+1.5V$	$V^+/-1.5V$ $V^-/+1.5V$
Slew Rate	4V/μs	0.5V/μs	2.5V/μs	3V/μs	0.3V/μs	0.1V/μs
GBW	1MHz	0.45MHz	3MHz	1MHz	0.8MHz	0.8MHz

*Unable to verify by laboratory testing. Measured at 0.7μVp-p.

**Measured at 5μVp-p in a 1Hz bandwidth.

Figure 1

particular concern with previous monolithic chopper designs and Figure 2 is a strip chart of the LTC1052's performance at two measurement bandwidths. Additionally, the LTC1052's input common-mode range includes V^-, making single-supply operation more practical.

Considerable attention to DC parasitics, particularly thermal EMFs, is required if the LTC1052's ultra low drift is to be fully utilized. Any connection of dissimilar metals produces a potential which varies with the junction's temperature (Seeback effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is probably the primary source of error. Connectors, switches, relay contacts, sockets, wire, and even solder are all candidates for thermal EMF generation. It is relatively clear that connectors and sockets can form thermal junctions. However, it is not at all obvious that junctions of wire from different manufacturers can easily generate 200nV/°C—four times the LTC1052's drift specification! Figure 3 shows a plot obtained for such a wire junction. Even solder can become an error term at low levels, creating a junction with copper or Kovar wires or PC traces (see Figure 4).

Minimizing thermal EMF induced errors is possible if judicious attention is given to circuit board layout. In general, it is good practice to limit the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and other potential error sources to the extent possible. In some cases this will not be possible.

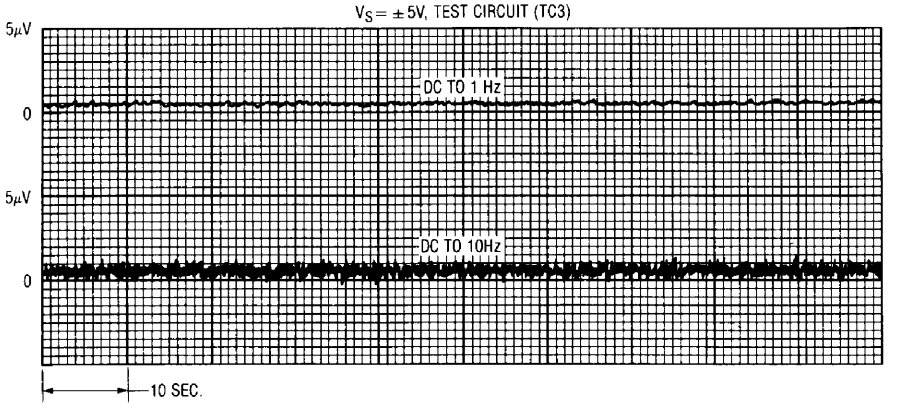

Figure 2 LTC1052 Input Noise Voltage

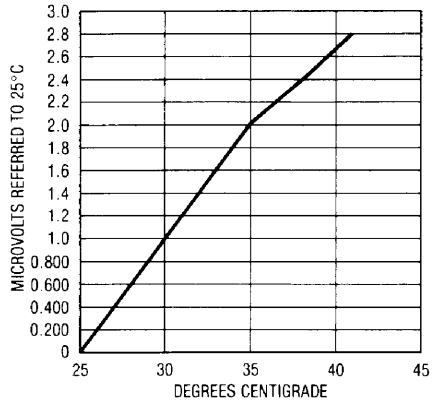

Figure 3. Thermal EMF Generated by Two Wires

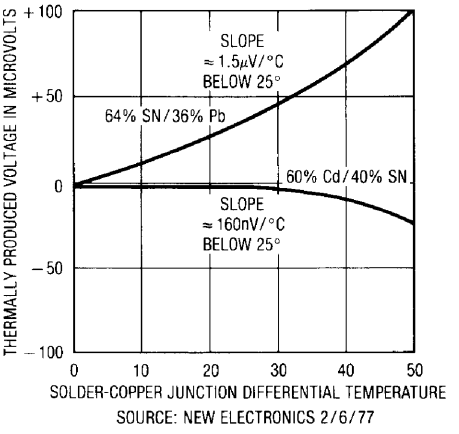

Figure 4. Solder-Copper Thermal EMFs

In these instances, attempt to balance the number and type of junctions in the amplifier inputs so that differential cancellation occurs. Doing this may involve deliberately creating and introducing junctions to offset unavoidable junctions. This practice, borrowed from standard lab procedures, can be quite effective in reducing thermal EMF originated drifts. Figure 5 shows a simple example where a nominally unnecessary resistor is included to promote such thermal balancing. For remote signal sources such as transducers, connectors may be unavoidable. In these cases choose a connector specified for relatively low thermal EMF activity and ensure a similarly balanced approach in routing signals through the connector, along the circuit board and to the amplifier. If some imbalance is unavoidable, deliberately introduce an intentional counterbalancing junction. In all cases maintain the junctions in close physical proximity, which will keep them at the same temperature. Avoid drafts and temperature gradients, which can introduce thermal imbalances and cause problems. Figure 6 shows the LTC1052 set up in a test circuit to measure its temperature stability. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity each input sees is also balanced because of the symmetrical connection of the resistors and their identical size. Thus, thermal EMF induced shifts are equal in phase and amplitude and cancellation occurs. Very slight air currents can still affect even this arrangement. Figure 7 shows strip charts of output noise with the circuit covered by a small styrofoam cup (HANDI-KUP Company Model H8-S) and with no cover in "still" air. This data illustrates why it is often prudent to enclose the LTC1052 and its attendant components inside some form of thermal baffle.

Thermal EMFs are the most likely, but not the only, potential low level error source. Electrostatic and electromagnetic shielding may be required. Power supply transformer fields are notorious sources of errors often mistakenly attributed to amplifier DC drift and noise. A transformer's magnetic field impinging on a PC trace can easily generate microvolts across that conductor in accordance with well-known magnetic theory. The amplifier cannot distinguish between this spurious signal and the desired input. Attempts to eliminate the problem by rolling off amplifier gain with a feedback capacitor may work, but often the filtered version of the undesired pickup masquerades as an unstable DC term in the output. The most direct approach is to use shielded transformers, but careful layout may be equally effective and less costly. A circuit which requires the transformer to be close by to achieve a good quality grounding scheme may be disturbed by the transformer's magnetic field. An RF choke connected across a scope probe can determine the presence and relative intensity of transformer fields, aiding layout experimentation.

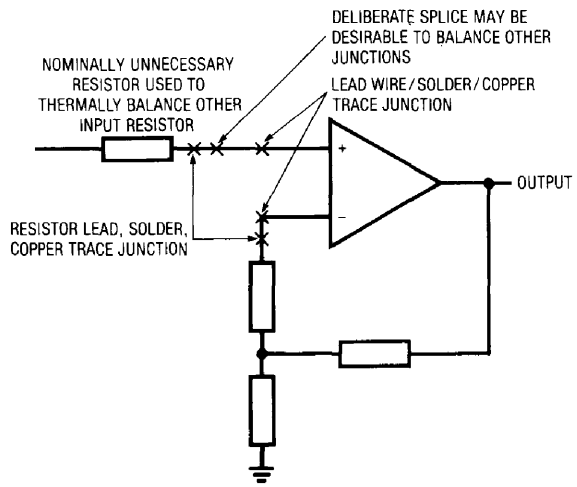

Figure 5. Typical Thermal Layout Considerations

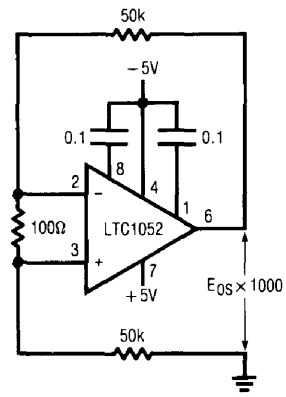

Figure 6. Recommended Drift Test Circuit

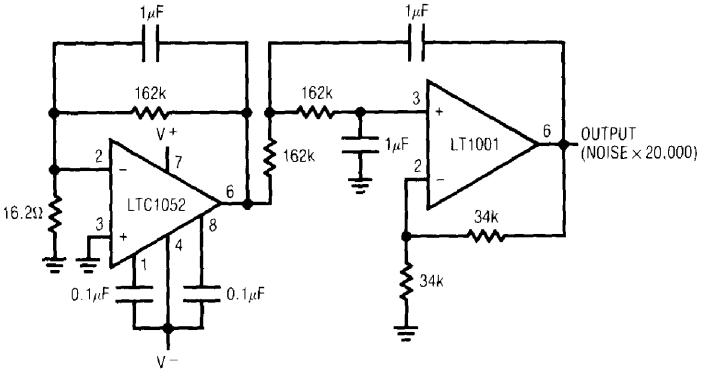

Figure 7. DC to 1Hz Noise Test Circuit

Another source of parasitic error is stray leakage current. The LTC1052's 30pA bias current allows operation from very high source impedances. In such cases it is desirable to prevent stray leakage currents from reaching the inputs. The simplest way to do this is to connect the amplifier inputs directly to the signal source via a teflon stand-off. Because the amplifier inputs never contact the PC board, stray leakage currents do not affect them. Although this approach is effective, its implementation may not be acceptable in production. Guarding is another technique to minimize board leakage effects. The guard is a PC trace completely encircling the input. This trace is driven (see Figure 8) at a potential equal to that of the input, preventing leakage to the amplifier input terminal. On PC boards, the guard should enclose the input(s) to be protected, with signal connections made directly to the amplifier input.

A final form of parasitic is one particular to all carrier-based amplifiers. If the amplifier is operating in a circuit which contains clocking or oscillation with substantial harmonic content at or near its carrier frequency (e.g., from another LTC1052), erratic operation is possible. This is particularly the case if inductors or transformers radiate magnetic fields related to the clocking or oscillation. The undesired interaction between the amplifier's chopping sequence and the externally generated AC signals may cause mixing and beat frequencies to occur, resulting in errors in the output. The LTC1052 is not particularly sensitive in this regard, but synchronizing its internal oscillator with external circuit clocking precludes this problem. The 14-pin version of the LTC1052 features a pin which allows the internal clock to be synchronized to an external signal. Input signals containing substantial AC content may also cause this problem if the AC signal

has strong spectral components related to the chopping frequency. In applications where such AC input components exist, it may be necessary to drive the LTC1052 from an external clock source at a frequency which has no harmonic relationship with the input signal. For example, a 372Hz clock frequency will prevent 60Hz input components from affecting amplifier operation.

Applications

Once alerted to the potential problems previously outlined, the engineer is prepared to design circuits around the LTC1052. The most obvious applications are at low level DC, where the low drift will improve performance over other amplifiers. More subtlely, it is possible to exploit the LTC1052's low offset uncertainties to extend the dynamic range of circuit operation. The circuits which follow demonstrate these points, using relatively straightforward examples of improvements in low level, precision performance. Additional, less obvious, circuits use the LTC1052 to stabilize and enhance the performance of a variety of functions including data converters, buffers and comparators.

Standard Grade Variable Voltage Reference

Figure 9 diagrams a standard lab grade variable voltage reference. This circuit combines a pair of LTC1052s with high grade saturated standard cells and other components to produce an extremely stable reference source. The circuit may be used to calibrate 6½ digit voltmeters, ultra high resolution data converters and other apparatus requiring high order traceability to primary standards.

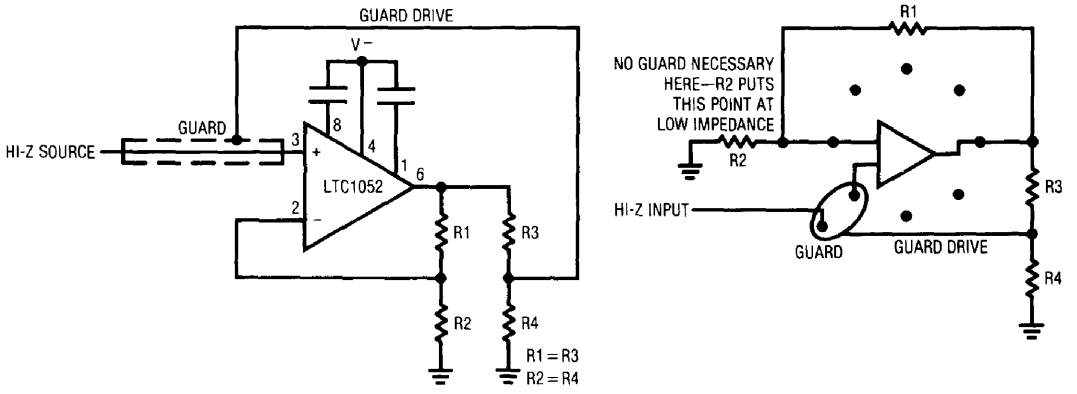

Figure 8. Guarding Technique and Typical Layout

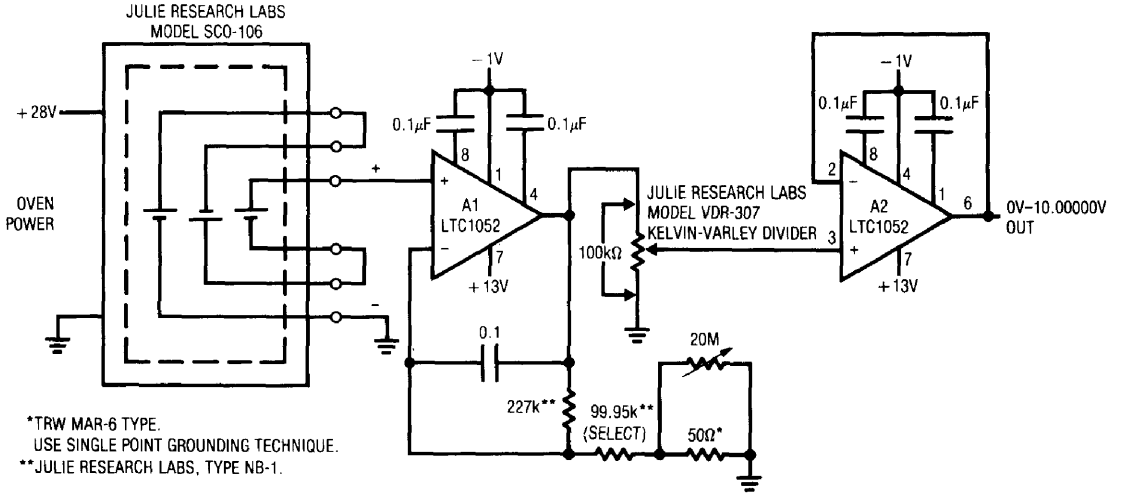

Figure 9. Standard Grade Variable Voltage Reference

The SCO-106 saturated cells furnish a reference voltage which is buffered and amplified to precisely 10V by A1. A1's output drives a seven place settable Kelvin-Varley divider with 1ppm accuracy. A2's low bias current and high CMRR allow it to unload the divider without introducing significant error. To calibrate this circuit, adjust A1's output for exactly 10V by selecting the feedback resistor and fine trimming the 20MΩ potentiometer. A1's output should be measured with equipment having order traceability to primary NBS standards. Once calibrated, this circuit will provide *worst-case* 0.0014% accuracy over one year's time and ±5°C temperature excursions. Figure 10 details error sources. Note that the amplifiers contribute only about 1.3ppm (0.00013%) of the total.

Ultra-Precision Instrumentation Amplifier

An ultra-precision instrumentation amplifier appears in Figure 11. This circuit offers greater accuracy and lower drift than any commercially available IC, hybrid or module.

SCO-106 Reference / 2ppm / Year		= 2ppm
A1 – 0.05μV/°C × A = 3 × 5°C = 0.75μV		= 0.075ppm
A2 – 0.05μV/°C × A = 1 × 5°C = 0.25μV		= 0.025ppm
A1 + A2 Time Drift / Year = 2μV		= 0.02ppm
KVD – 0.5ppm/°C × 5°C + 1ppm/Year = 3.5ppm		= 3.5ppm
Resistors – 0.1ppm/°C Ratio 5°C + 2ppm/Year = 2.5ppm		= 2.5ppm
A2 CMRR Error	= 1ppm 1.2ppm	= 1.2ppm
A2 Loading Error	= 0.2ppm	9.32ppm

Figure 10. Error Sources for Ultra-Precision Voltage Reference

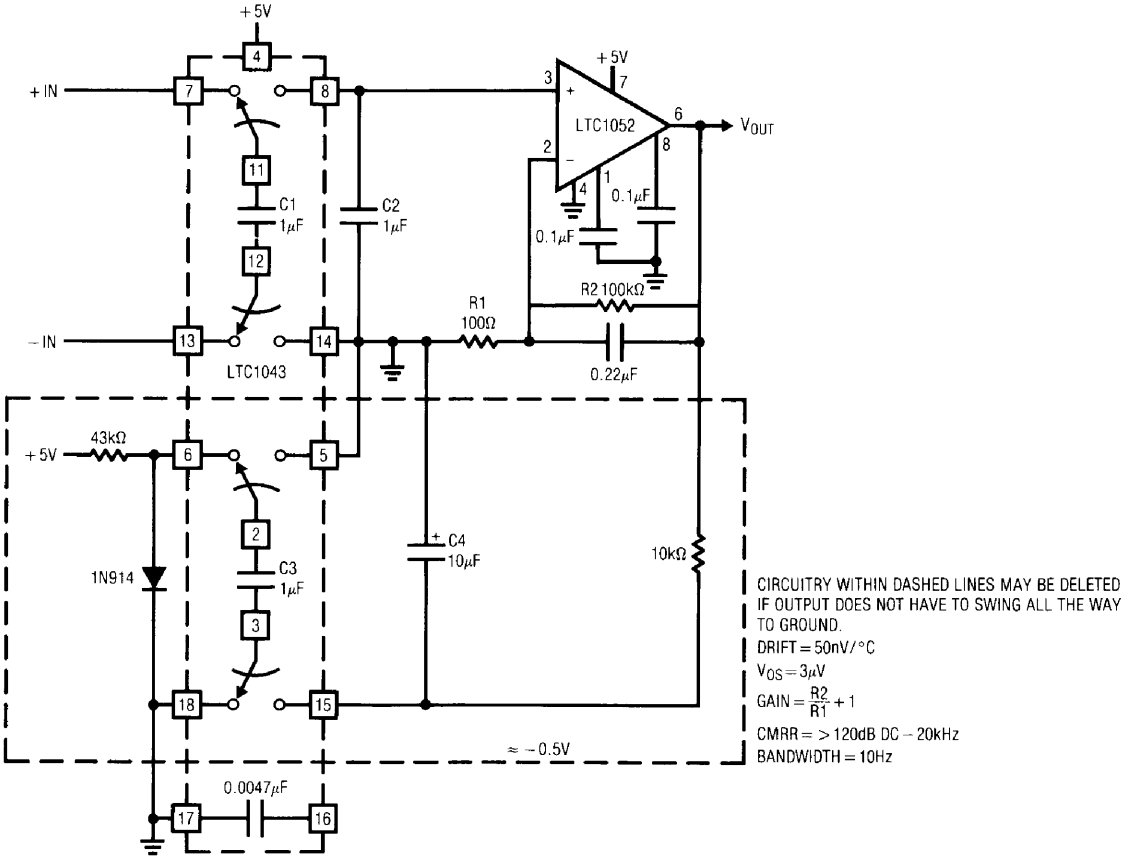

Figure 11. Ultra-Precision Instrumentation Amp

Additionally, it will run from a single 5V power supply. The LTC1043 switched-capacitor instrumentation building block provides a differential-to-single-ended transition using a flying capacitor technique. C1 alternately samples the differential input signal and charges ground referred C2 with this information. The LTC1052 measures the voltage across C2 and provides the circuit's output. Gain is set by the ratio of the amplifier's feedback resistors. Normally, the LTC1052's output stage can swing within 15mV of ground. If operation all the way to zero is required, the circuit shown in dashed lines may be employed. This configuration uses the remaining LTC1043 section to generate a small negative voltage by inverting the diode drop. This potential drives the 10kΩ pull-down resistor, forcing the LTC1052's output into class A operation for voltages near zero. Note that the circuit's switched-capacitor front end forms a sampled data filter allowing common-mode rejection ratio to remain high, even with increasing frequency. The 0.0047μF unit sets front end switching frequency at a few hundred hertz. The chart details circuit performance.

High Performance Isolation Amplifier

Instrumentation amplifiers cannot be used to signal condition all differential signals. In factory and process control environments, severe grounding and common-mode voltages often mandate the requirement for isolation amplifiers. Isolation amplifiers feature inputs which are galvanically isolated from their output and power connections. This allows the amplifier to ignore the effects of ground loops and operate at input common-mode voltages many times the power supply voltage. Implementing a precise, low drift isolation amplifier is not easy, and commercial units are quite expensive. Figure 12 shows a circuit with 0.03% transfer accuracy and the 50nV/°C input drift of the LTC1052. As shown, the circuit provides a gain of 1000 and will operate at 250V input common-mode levels.

The circuit works by amplitude modulating the output of a signal conditioning amplifier through a transformer. A synchronous demodulator filter reconstructs the amplifier's original output and furnishes the circuit's output. A separate oscillator and transfomer provide power to the amplifier, preserving galvanic isolation between the circuit's input and output ports.

Three 74C04 gates and their associated components form an oscillator which provides complementary drive to Q5 and Q6. These devices energize L1, which generates floating power on the input side of the dashed barrier shown. Simultaneously, the oscillator provides slightly delayed complementary drive to the Q1–Q2 FET switches via the 330Ω-100pF network and the additional inverters. The floating power produced by L1 is rectified and filtered and drives the LTC1052 (A1) via the zener drops of the transistors. The ± 15V floating power is brought out so it can be used to power transducers or other loads. Interaction between the transformer's chopping carrier and A1's internal oscillator is avoided by synchronizing the amplifier to the carrier via the two decade counters. Q3 and Q4, driven by opposing phase carrier signals derived from L1, chop A1's output into L2. This modulated signal information is received at L2's other winding. Because Q1 and Q2 are driven synchronously with Q3 and Q4, they demodulate the amplitude and phase (e.g., plus or minus polarity) information in the carrier. The 330Ω–100pF network compensates for the slight skew in switch drive signals on opposing sides of L2, minimizing gain error. L2's output (pin 2) is RC filtered at A2, which also provides the circuit's output. Slight switching errors in the modulator-demodulator result in very small gain differences between positive and negative outputs at pin 2 of L2. This effect is compensated by the diode-resistor network in A2's output, which provides a small decrease in gain for negative outputs.

Figure 13 shows the response of the isolation amplifier to a sine wave input. For this test, the floating common and circuit grounds are tied together. Trace A is the input applied to A1. Trace B, taken at pin 4 of L2, shows A1's amplified output being modulated into the transformer. Trace C, obtained at pin 1 of L2, depicts the received modulated waveform as it is synchronously demodulated. The filtered and final output of A2 appears in Trace D. The 25kHz carrier limits full power bandwidth of this circuit to about 500Hz, adequate for process control and transducer applications. The transformers used set a voltage breakdown specification of 250V, although higher levels are achievable with different devices. As shown, circuit gain is 1000, allowing amplification of a ± 5mV signal riding on 250V of common-mode to a ± 5V output. Gain accuracy is 0.03% with a gain drift of typically 50ppm/°C. Input referred drift is set by the LTC1052's 50nV/°C specification.

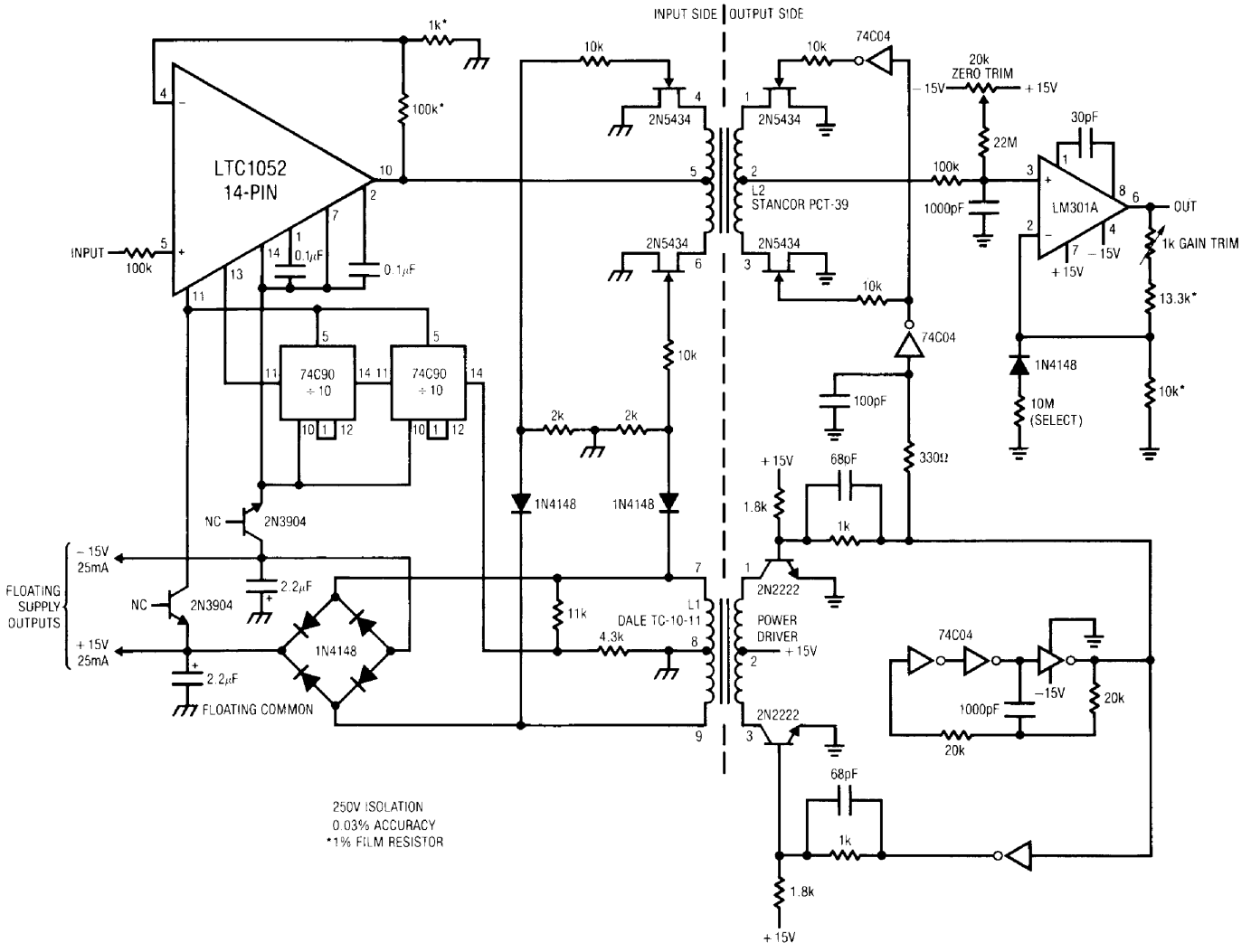

Figure 12. Precision Isolation Amplifier

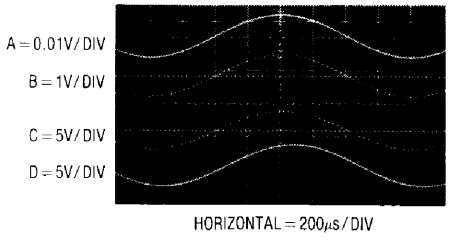

Figure 13. Waveforms for Isolation Amplifier

To trim this circuit, tie A1's input to floating common and adjust the zero trim for 0V output. Next, connect A1's input to a +5mV source and adjust the gain trim at A2 for exactly $+5.000V_{OUT}$. Finally, connect A1's input to a −5mV source and select the 10MΩ value in A2's feedback path for a −5.000V output reading. Repeat this procedure until all three points are fixed.

Stabilized, Low Input Capacitance Buffer (FET Probe)

A recurring requirement in automatic semiconductor testing and probing equipment is for a highly stable unity-gain buffer amplifier with low input capacitance. Such an amplifier is also useful for other circuit chores where it is desirable to accurately monitor a point without introducing any significant AC or DC loading terms. Figure 14 shows such a circuit. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open loop configuration would be quite drifty because there is no DC feedback. The LTC1052 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The diode in Q1's source line ensures that the gate never forward biases and the 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

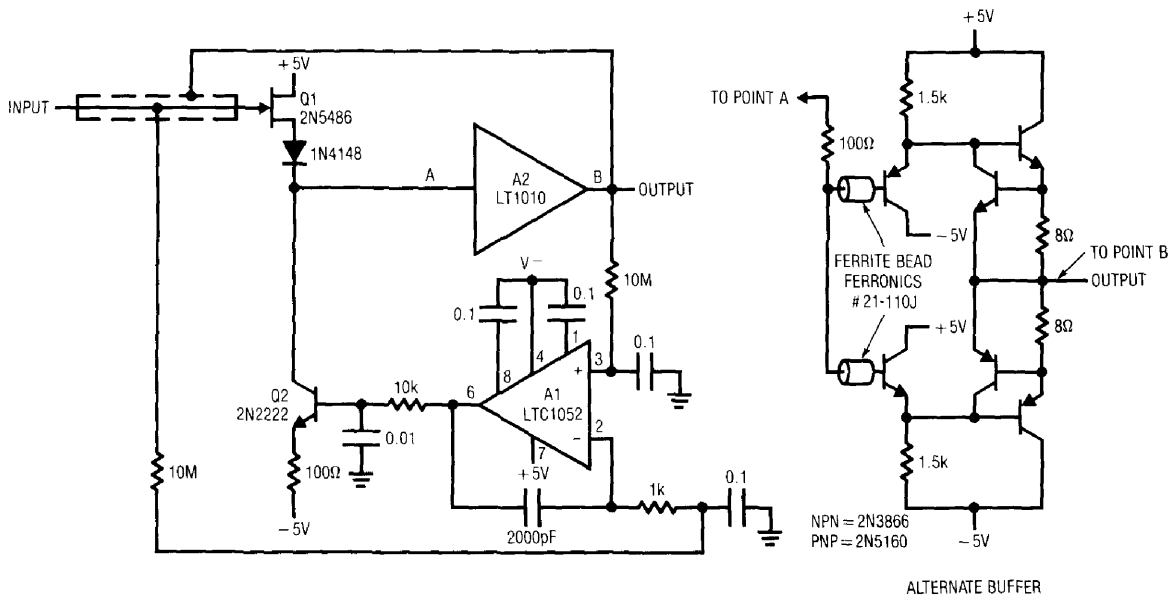

Figure 14. Fast, Stabilized FET Buffer

The LT1010's 15MHz bandwidth and 100V/μs slew rate, combined with its 150mA output, are fast enough for most circuits. For very fast requirements, the alternate discrete component buffer shown will be useful. Although its output is current limited at 75mA, the GHz range transistors employed provide exceptionally wide bandwidth, fast slewing and very little delay. Figure 15 shows the LTC1052 stabilized buffer circuit's response using the discrete stage. Response is clean and quick, with delay inside 4ns. Note that rise time is limited by the pulse generator and not the circuit. For either stage, offset is set by the LTC1052 at 3μV, with gain about 0.95. It is worth noting that this circuit performs the same function as commercial FET probes in the $1,000.00 range.

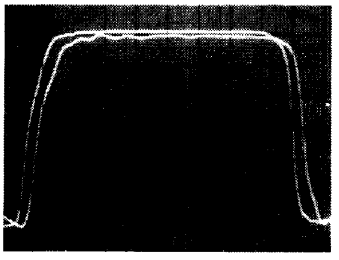

Figure 15. Stabilized Buffer Delay

Chopper-Stabilized Comparator

It is often desirable to use a reasonably fast voltage comparator with low input offset drift. Such a device is useful in high resolution A→D converters, crossing detectors and anywhere else a precise, stable, high speed comparison must be made. Unfortunately, obtaining reasonable comparator speed and low input drift in a design is difficult and monolithic comparators must be constructed around this trade-off. Figure 16 shows a way to use the LTC1052 to eliminate offset and drift in a comparator without sacrificing speed or differential input versatility. This circuit is applicable only in situations where some dead time is available for zeroing action to occur.

The circuit functions by periodically shorting the comparator inputs together and forcing the comparator into its linear region via its offset pins. The voltage at the offset pins required to do this is stored. When the comparator inputs are returned to their normal states, the stored voltage is maintained at the comparator's offset pins, effectively controlling the device's offset. Periodic updating ensures long term stability of the correction. In this circuit, A1 is the stabilizing amplifier for C1. C1's inputs are controlled by a dual DPDT switch section furnished by the LTC1043. When LTC1043 pin 16 is high, pins 12 and 11 are connected to pins 13 and 7, respectively. Pin 3, at C1's output, is connected to pin 18. Under these conditions, A1 is effectively connected in a negative feedback loop between C1's output and its offset pin 5 (see detail of LT1011 input stage in Figure 16). This forces C1 into its linear region and its output oscillates at a high frequency between the rail voltages. A1, connected as a low frequency integrator, filters this action, compares its DC equivalent value to ground (its positive input potential) and drives C1's offsets to zero. When pin 16 of the LTC1043 goes low, all switch states reverse and C1's inputs are free to compare the signals present at LTC1043 pins 14 and 8 in the normal fashion. During this interval, A1's output remains fixed at the voltage stored in its feedback capacitor. A1's low bias current allows long durations between correction cycles—periods of seconds are practical—while maintaining effective comparator offset well within 5μV with negligible temperature drift.

Figure 17 shows the circuit's response to a sine wave (Trace A) applied to C1's positive input at LTC1043 pin 14. C1's negative input, LTC1043 pin 8, is grounded. With the circuit's zero command low (Trace B), C1's output (Trace C) responds in the normal fashion. During this period, the status output (Trace D) is low, indicating C1 is in its normal mode. When the zero command occurs (Trace B, just to the right-center of the screen), C1 is forced into its linear region, where it oscillates. During this time, A1 updates the correction voltage stored in its feedback capacitor. When the zero command pulse falls, normal comparator action is seen to resume. Note that the circuit's status output reflects the true operating mode of the circuit, because its timing includes the 50ns delay of the LTC1043 switch. For this reason the status output, and not the zero command, should be used to indicate the circuit's actual operating state.

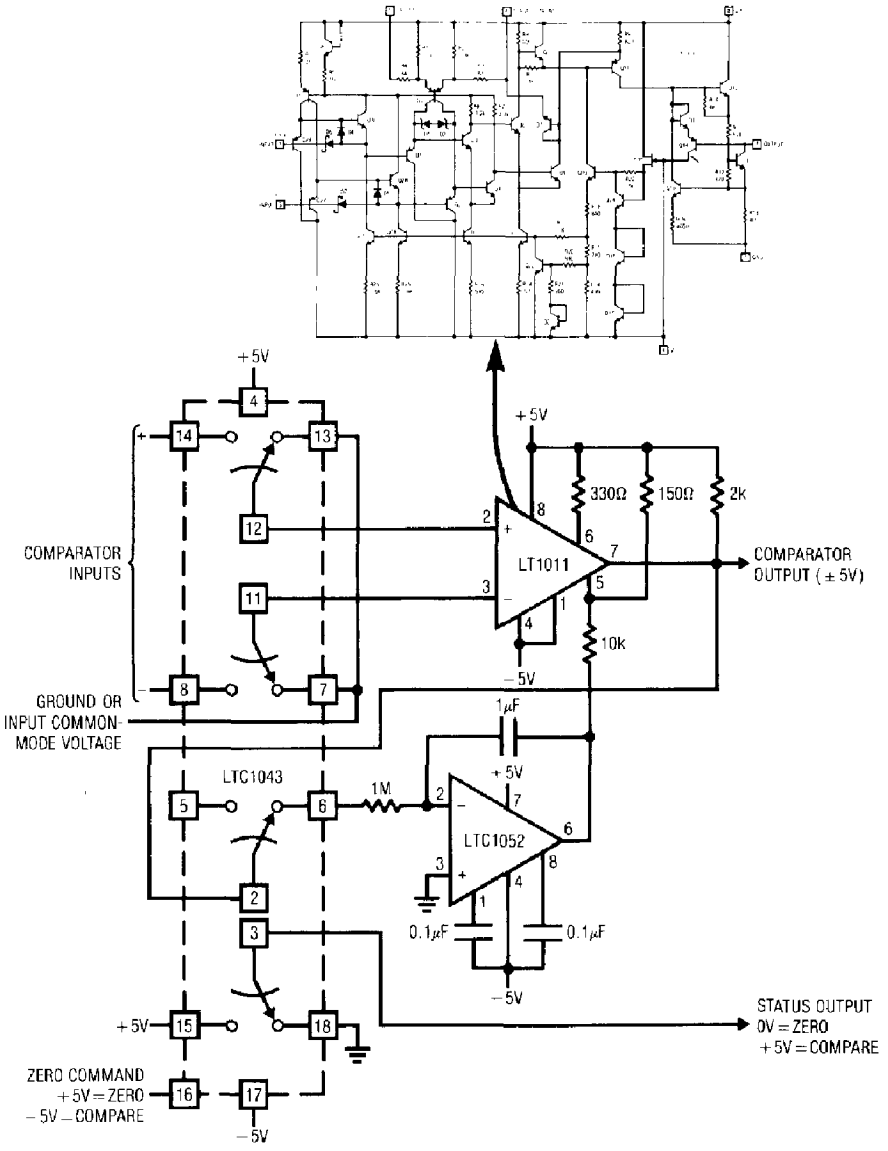

Figure 16. Offset Stabilized Comparator

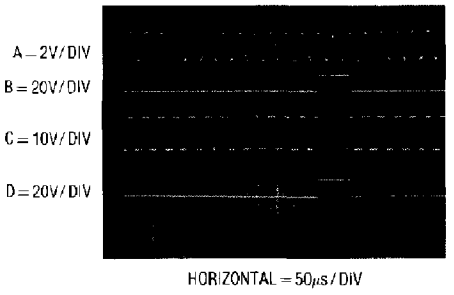

Figure 17. Stabilized Comparator Waveforms

Stabilized Data Converter

Amplifiers and comparators are not the only elements which can benefit from chopper-stabilization by the LTC1052. Figure 18 shows a way to offset-stabilize a data converter, thereby doubling its dynamic range of operation, eliminating the necessity for an offset trim and reducing zero drift to negligible levels. In this circuit, the LTC1052 corrects for offset deficiencies in the AD650 V→F converter. Although specified for 1MHz full-scale operation, this device's 4mV input offset limits untrimmed dynamic range of operation to only 3½ decades of output frequency. Under normal operating conditions, the AD650's positive input is grounded and its negative input is driven via the resistor string shown. Obtaining more than 3½ decades of operation requires an offset trim at pins 13 and 14. Even after trimming, the input amplifier's 30μV/°C drift contributes a 3Hz/°C zero point error. The LTC1052 corrects these problems by measuring the offset voltage at the circuit's summing node, comparing it to ground and driving the AD650 positive input (normally grounded in the manufacturer's recommended circuit configuration) with the appropriate stabilizing correction voltage. The dual FETs eliminate bias current caused errors. The LTC1052's integrator configuration keeps its gain at low frequency and DC, preserving the AD650's fast dynamic response while eliminating its offset errors. The divider network in the LTC1052's output is scaled to allow enough correction range to zero the AD650's offsets without causing overdrive during start-up and transients. With this scheme in use, the circuit does not require any zero trim to achieve full 6 decade operation. To calibrate, apply 10V and trim the output for exactly 1MHz.

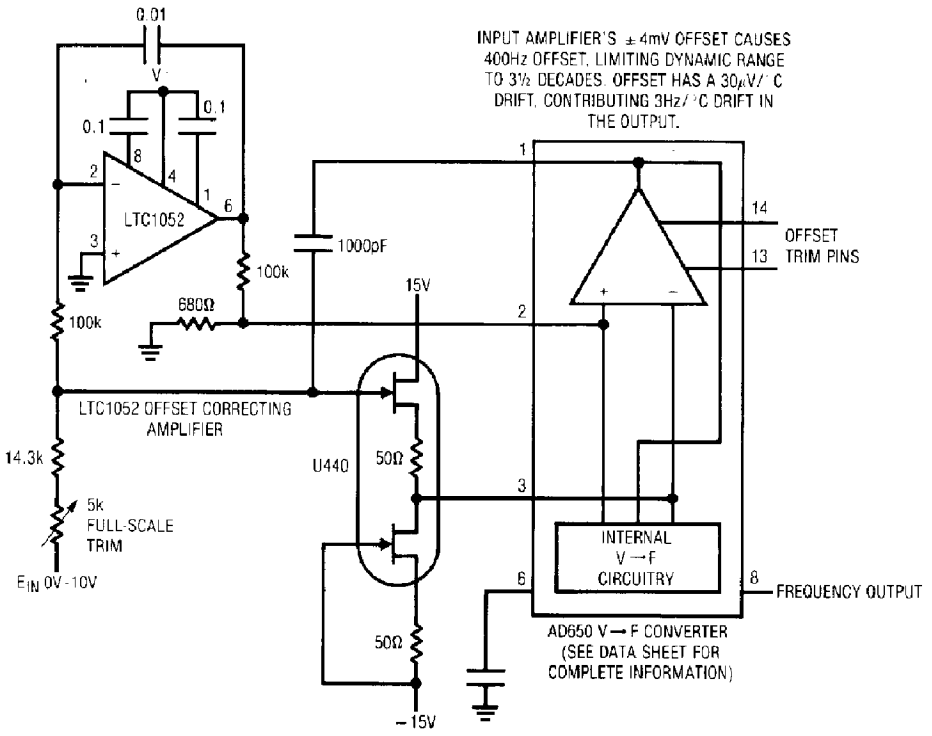

Figure 18. Offset Stabilizing a V→F Converter

Wide Range V→F Converter

Figure 19 shows another stabilized V→F converter. It features 1Hz–1.25MHz operation, 0.05% linearity, and a temperature coefficient of typically 20ppm/°C, all substantially better than Figure 18's circuit. Additionally, it is less expensive and runs from a single 5V supply. Tradeoffs include slower step response and a larger component count. This circuit uses a charge feedback scheme to allow the LTC1052 to close a loop around the entire V→F converter, instead of simply controlling offset. This approach enhances linearity and stability but introduces the loop's settling time into the overall V→F step response characteristic. Figure 20 shows waveforms of operation.

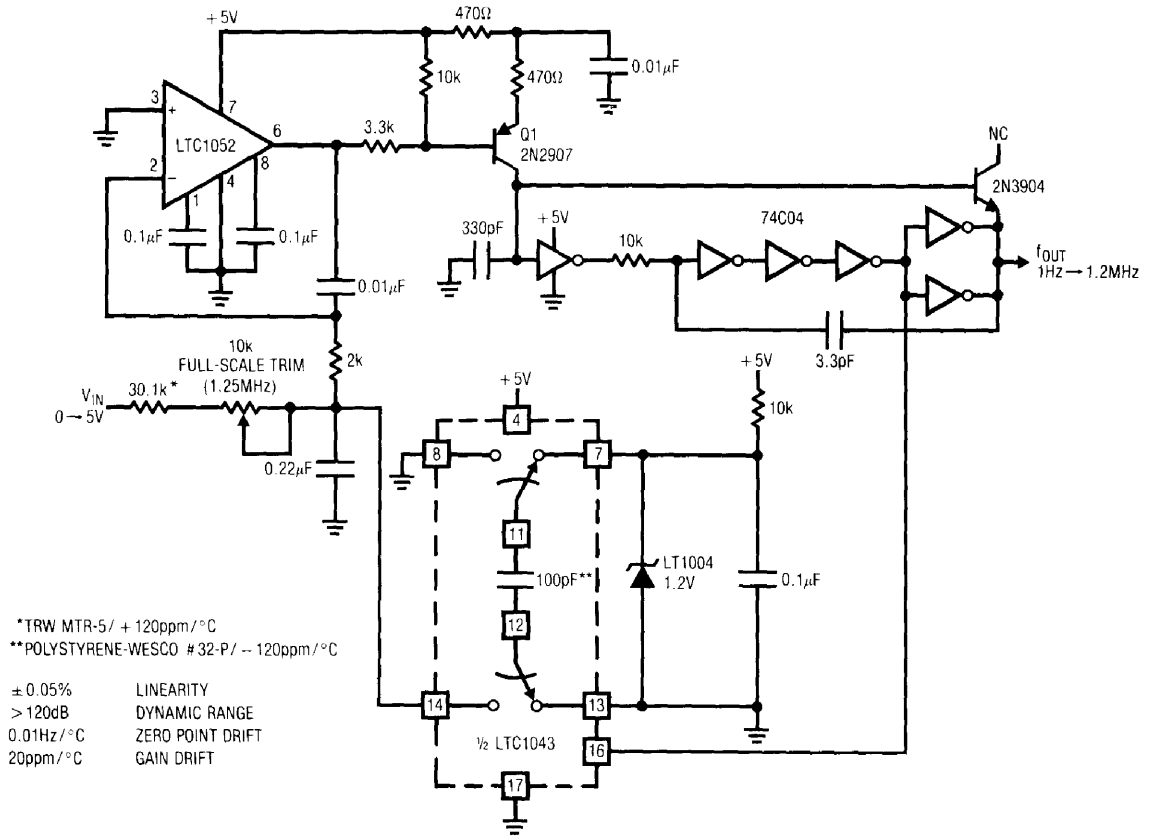

Figure 19. 1Hz–1.25MHz Voltage-to-Frequency Converter

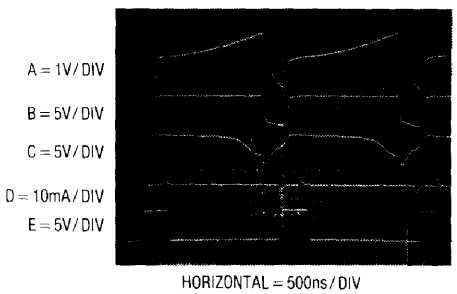

Figure 20. V→F Waveforms

A positive input voltage directs A1's output to go negative, biasing the Q1 current source. Q1's collector puts current into the 330pF capacitor, causing it to rise in voltage (Trace A, Figure 20). The low input current CMOS inverter changes state when the ramp crosses ½ of the supply voltage. This causes all of the inverters to switch. The two paralleled inverters at the end of the chain go low (Trace B), simultaneously supplying positive feedback at the 10k-3.3pF junction (Trace C) and forcing the 330pF capacitor to a lower voltage by removing current from it (Trace D) via the diode connected 2N3904. During the ramping interval, LTC1043 switch pins 11 and 12 are connected to pins 8 and 14 discharging the 100pF capacitor into pin 14. When the output inverters go low, the LTC1043's control pin (16) also switches, placing the charged 100pF capacitor across pins 7 and 13. Thus, each time the inverters switch, a fixed quantity of charge is dispensed into the 2k-0.22μF-10k potentiometer junction (Q = CV). The LTC1043's switching is arranged so that this charge is of opposite polarity to the positive input current. The 0.22μF capacitor integrates the discrete charge dumps to DC. A1 servo controls the Q1 inverter oscillator to run at whatever frequency is required to force its negative input to 0V. In this manner, drift and non-linear response in the Q1 inverter oscillator are compensated by A1's closed loop control. The circuit's frequency output is delivered by another LTC1043 section (Trace E).

Several factors contribute to this circuit's performance. The low input current of the CMOS inverter, combined with the low leakage of the 2N3904 base-emitter diode and the circuit's servo action, allows operation to well below 1Hz, despite the small 330pF integrating capacitor. In the lower frequency ranges, currents at this junction are small and board leakage can cause jitter. A clean board will work well, but the best approach is to mount the capacitor, Q1's collector, the inverter input and the transistor base connection on a teflon stand-off, using short connections. The resistor and capacitor specified in the figure, both gain terms, have opposing temperature coefficients, aiding gain drift performance. The LTC1052's low offset eliminates the need for a zero trim while preserving the circuit's >120dB dynamic range of operation. To trim the circuit, apply +5.000V and adjust the 1.25MHz trim for 1.2500MHz out.

1Hz-30MHz V→F Converter

Although Figure 19's circuit is impressive, it still does not tax the LTC1052's dynamic range of operation. Figure 21 shows a highly modified version of Figure 19. It has a 1Hz to 30MHz output (150dB dynamic range) for a 0V to 3V input. This is by far the widest dynamic range and highest operating frequency of any V→F discussed in the literature at the time of writing*. It is a good application of the extremely wide signal processing range afforded by the LTC1052. The circuit maintains 0.08% linearity over its entire 7⅓ decade range with a full-scale drift of about 20ppm/°C. Zero point error is 0.3Hz/°C and is directly related to the LTC1052's 50nV/°C drift specification.

To get the additional bandwidth, Figure 19's CMOS inverters are replaced with a fast JFET buffer driving a Schottky TTL Schmitt trigger. The Schottky diode prevents the Schmitt trigger from ever seeing negative voltage at its input. The diode connected 2N3904 is retained for resetting the capacitor, which has a smaller value. Figure 19's positive AC feedback, with its attendant recovery time constant, is avoided in this circuit. Instead, the Schmitt's input voltage hysteresis provides the limits which the oscillator runs between. The 30MHz full-scale output is much faster than the LTC1043 can accept, so the digital divider stages are used to reduce the feedback frequency signal by a factor of 20. Remaining Schmitt sections furnish complementary outputs. Good high frequency wiring techniques should be used when constructing the current source-buffer-Schmitt trigger sections.

Figure 22 shows the key waveforms with the circuit loafing at 20MHz. Trace A is the Schmitt trigger input, which is seen to ramp between two voltage limits, while Trace B is the Schmitt output. The closed loop approach results in very low output jitter and noise over the entire 150dB operating range. Figure 23 plots this, showing frequency jitter versus output frequency. Jitter does not rise above 0.01% until 20kHz, which is only 0.05% of scale. Even at 1ppm of scale (30Hz), jitter is still about 1%, finally rising to 10% at 1Hz (0.000003% of full-scale). As V→F operating frequency decreases toward the LTC1052's feedback loop roll-off, the loop dominates the jitter characteristic. In the high frequency ranges the loop

*1Hz–100MHz circuit is under development and will be discussed in AN-14, "Designs for High Performance V→F Converters."

poles are not a factor and current source and Schmitt trigger switching noise dominate. As with Figure 19's circuit, the feedback loop slows step response. Figure 24 shows this, with a full-scale input step requiring almost 50ms to settle. To trim this circuit, ground the input and adjust the 1Hz trim until oscillation just starts. Next, apply 3.000V and set the 30MHz trim for a 30.00MHz output. Repeat this procedure until both points are fixed.

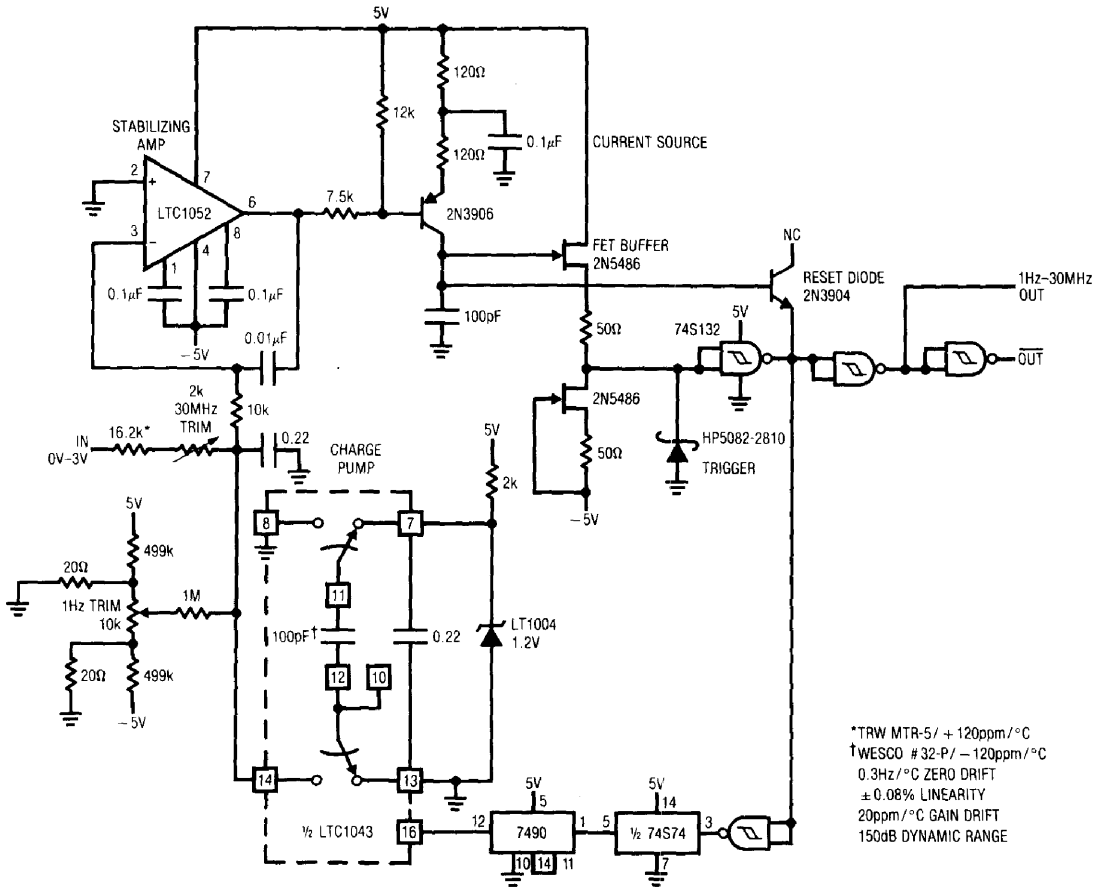

Figure 21. 1Hz-30MHz V → F Converter

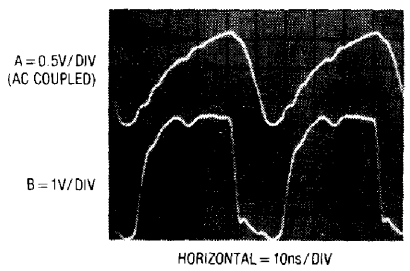

Figure 22. Fast V → F Ramp-Reset Detail

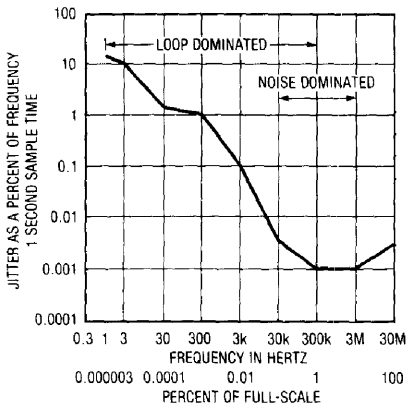

Figure 23

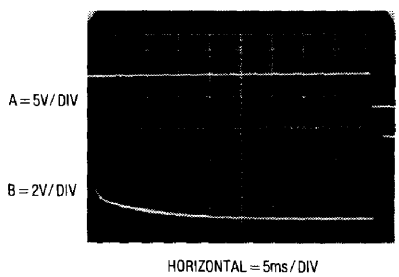

Figure 24. Fast V → F Step Response

16-Bit A→D Converter

V→F converters are not the only types of data converters which can benefit from the LTC1052's performance. Figure 25 shows a 16-bit A→D converter (overrange to 100,000 counts is provided).

The A→D converter, made up of A2, a flip-flop, some gates and a current sink, is based on a current balancing technique. Once again, the chopper-stabilized LTC1052's 50nV/°C input drift is required to eliminate offset errors in the A→D. Figure 26 details key A→D waveforms. Assume the flip-flop's Q output (Trace B) is low, connecting LTC1043 pins 3 and 18. The current sink switch directs its output to ground.

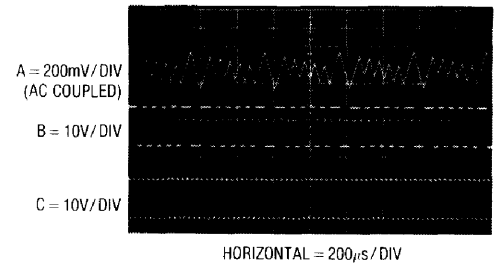

Figure 26. 16-Bit A→D Waveforms

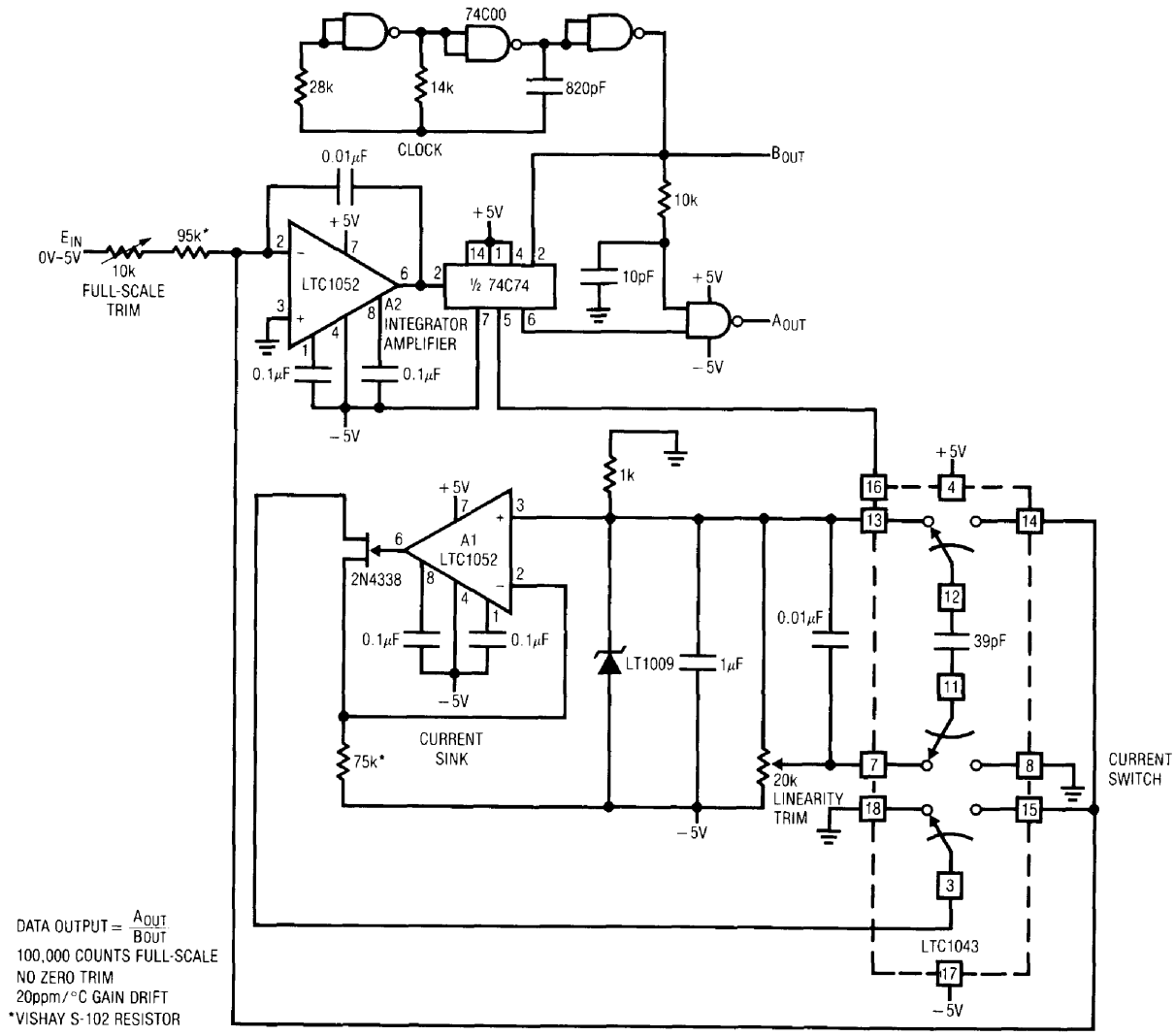

Figure 25. 16-Bit A→D Converter

Under these conditions, the only current into A2's summing point is from the input via the 95kΩ resistor. This positive current forces A2's output (Trace A, Figure 26) to integrate in a negative direction. The negative ramp continues and finally passes the 74C74 flip-flop's switching threshold. At the next clock pulse (clock is Trace C), the flip-flop changes state (Trace B), causing the LTC1043 switch positions to reverse. Pin 3 connects to pin 15, allowing the current sink to bias A2's summing point.

This results in a quickly rising, precise current flow out of A2's summing point. This current, scaled to be greater than the maximum input derived current, forces A2's output movement to reverse and integrate in the positive direction. At the first clock pulse after A2's output has crossed the flip-flop's triggering threshold, switching occurs and the entire cycle repeats. Because the reference current is fixed, the flip-flop's duty cycle is solely a function of the input signal current into A2's summing point. The flip-flop's output gates the clock, producing the "frequency output A" output. The 10k-10pF RC slightly delays the clock signal, eliminating spurious output pulses due to flip-flop delay. The circuit's data output, the ratio of output A to the clock frequency, may be extracted with counters. Because the output is expressed as a ratio, clock frequency stability is unimportant.

Slight parasitic charge pumping at the current switch introduces an error term which varies with loop operating frequency. This effect will cause a small nonlinearity in the A→D's transfer function unless compensated. The remaining LTC1043 sections accomplish this by inverting the reference and returning a very small, compensatory charge to the current sink output each time circuit switching occurs. The charge delivered is scaled by the linearity trim to cancel the parasitic term. To calibrate this circuit, apply 5.00000V and adjust the full-scale trim for 100,000 counts out. Next, set the input to 1.25000V and adjust the linearity trim for 25,000 counts out. Repeat this procedure until both points are fixed. Converter accuracy is ±1 count with a temperature coefficient of typically 15ppm/°C. Better TC is possible by employing a more stable reference. The high offset stability of the LTC1052 at A2 eliminates zero errors and trimming.

Simple Remote Thermometer

Although many remote thermometer circuits have appeared, few allow the temperature transducer's output to be directly transmitted over an unshielded wire. The relatively high output impedance of most temperature transducers makes their outputs sensitive to noise on the line and shielding is required. The low offset drift of the LTC1052 permits the circuit of Figure 27, which offers one solution to this problem. Here, the low output impedance of a closed loop op amp gives ideal line-noise immunity, while the op amp's offset voltage drift provides a temperature sensor. Using the op amp in this way requires no external components and has the additional advantages of a hermetic package and unit-to-unit mechanical uniformity if replacement is ever required.

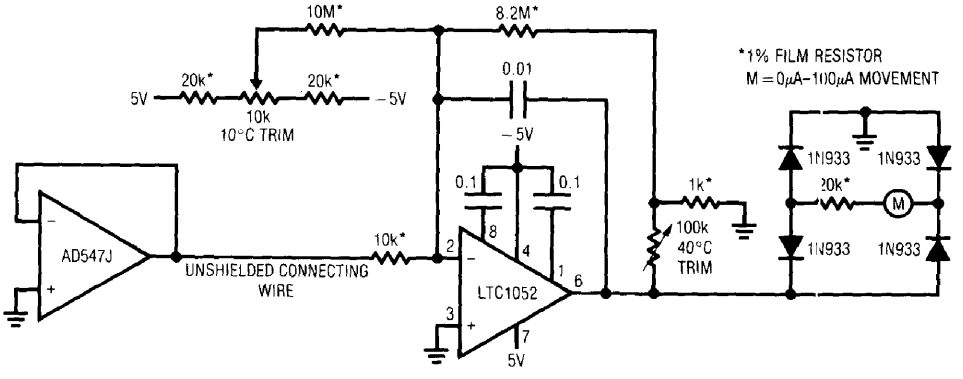

Figure 27. High Noise Rejection Thermometer

The op amp's offset drift is amplified to drive the meter by the LTC1052. The diode bridge connection allows either positive or negative op amp temperature sensor offsets to interface directly with the circuit. In this case, the circuit is arranged for a +10°C to +40°C output, although other ranges are easily accommodated. To calibrate this circuit, subject the op amp sensor to a +10°C environment and adjust the 10°C trim for an appropriate meter indication. Next, place the op amp sensor in a +40°C environment and trim the 40°C adjustment for the proper reading. Repeat this procedure until both points are fixed. Once calibrated, this circuit will typically provide accuracy within ±2°C, even in high noise environments.

Output Stages

In some circumstances it may be required to obtain more output current or swing from the LTC1052 than it can provide. The CMOS output stage cannot provide the current levels of bipolar op amps. Additionally, it may be necessary to run the device off ±15V supplies and to obtain increased voltage and current outputs. Figure 28 parallels a package of CMOS inverters to obtain 10mA–20mA output current capability. The inversion in the loop requires the feedback connection to go to the amplifier's positive input. The RC damper eliminates oscillation in the inverter stage, which is running in its linear region. The local capacitive feedback at the amplifier gives loop compensation. Figure 29 shows a way to run the LTC1052 from +15V supplies while obtaining the increased current and voltage output capabilities of the LT318A amplifier. The transistors run in zener mode, dropping the supply to about ±7V at the LTC1052. The LT318A serves as an output stage with a voltage gain of 4. The output swing is that of the LT318A, typically, ±13V into 2kΩ with a short circuit current of 20mA. This circuit is dynamically stable at any gain in either the inverting or noninverting configuration, although the LTC1052's input common-mode range (−7V to +5V with the ±15V power supply used) must not be exceeded.

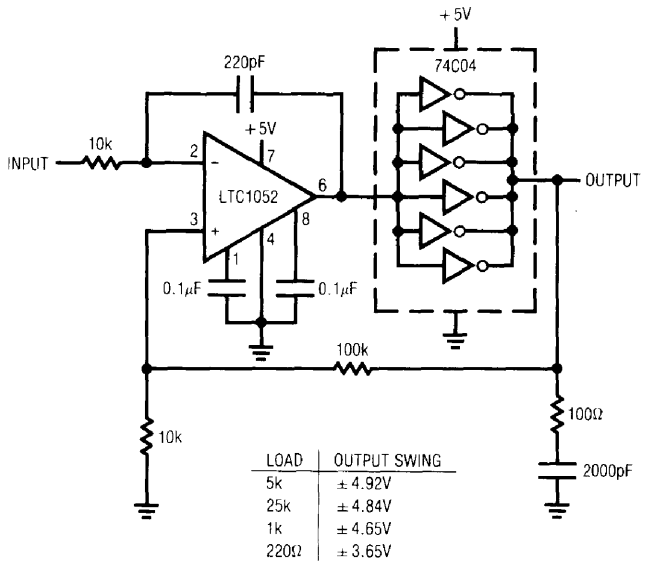

Figure 28. Increasing Output Current

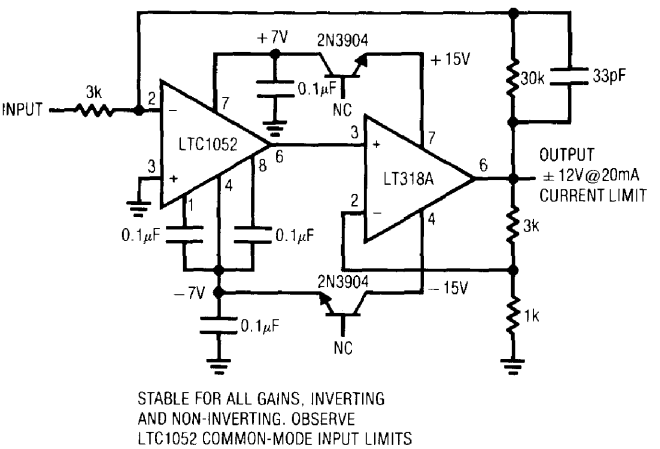

Figure 29. Increasing Output Current and Voltage (V_{SUPPLY} = ±15V)

Box Section—Choppers, Chopper-Stabilization and the LTC1052

All chopper-stabilized amplifiers achieve high DC stability by converting the DC input into an AC signal. An AC gain stage amplifies this signal. After amplification it is converted back to DC and presented as the amplifier's output. Figure B1 shows a conceptual chopper amplifier.

The AC amplifier's input is alternately switched between the signal input and the feedback divider network. The AC amplifier's output amplitude represents the difference between the feedback signal and the circuit's input. This output is converted back to DC by a phase sensitive demodulator composed of a second switch, synchronously driven with the input switch. The output integrator stage smooths the switch output to DC and presents the final output. Drifts in the output integrator stage are of little consequence because they are preceded by the AC gain stage. The DC drifts in the AC stage are also irrelevant because they are isolated from the rest of the amplifier by the coupling capacitors. Overall DC gain is extremely high, being the product of the gains of the AC stage and the DC gain of the integrator. Although this approach easily yields drifts of 100nV/°C and open loop gains of 100 million, there are some drawbacks. The amplifier has a single-ended, non-inverting input and cannot accept differential signals without additional circuitry added at the front end. Also, the carrier-based approach constitutes a sampled data system and overall amplifier bandwidth is limited to a small fraction of the carrier frequency. Carrier frequency, in turn, is restricted by AC amplifier gain-phase limitations and errors induced by switch response time. Maintaining good DC performance involves keeping the effects of these considerations small and carrier frequencies are usually in the low kilohertz range, dictating low overall bandwidth.

The classic chopper-stabilized amplifier solves the chopper amplifier's low bandwidth problem. It uses a parallel path approach (Figure B2) to provide wider bandwidth while maintaining good DC characteristics. The stabilizing amplifier, a chopper type, biases the fast amplifier's positive terminal to force the summing point to zero. Fast signals directly drive the AC amplifier, while slow ones are handled by the stabilizing chopper amplifier. The low frequency cut-off of the fast amplifier must coincide with the high frequency roll-off of the stabilizing amplifier to achieve smooth overall gain-frequency characteristics. With proper design, the chopper-stabilized approach yields bandwidths of several megahertz with the low drift characteristic of the chopper amplifier. Unfortunately, because the stabilizing amplifier controls the fast amplifier's positive terminal, the classic chopper-stabilized approach is restricted to inverting operation only.

The LTC1052 uses a different approach which permits full differential input operation, good bandwidth and retains ultra-low drift. It relies on an auto-zero technique.

During the LTC1052's auto-zero cycle, the inputs are shorted together and a feedback path is closed around

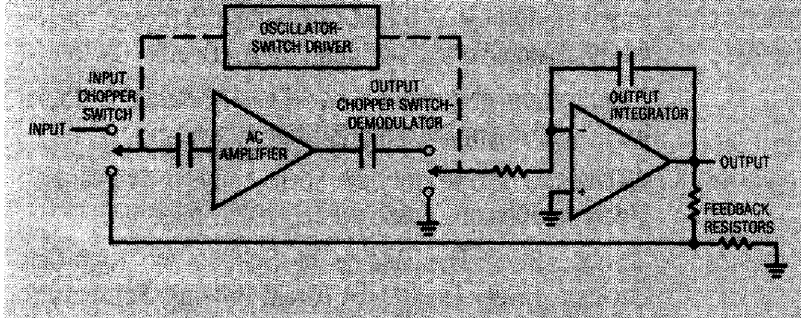

Figure B1. Chopper Amplifier

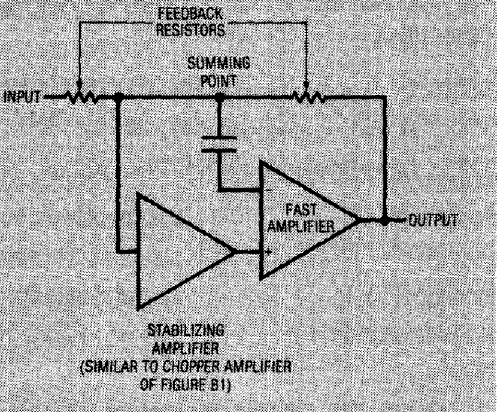

Figure B2. Classic Chopper-Stabilized Amp

the input stage to null its offset. Switch S2 (Figure B3) and capacitor C_{EXT} A act as a sample and hold to store the nulling voltage during the sampling cycle.

In the sampling cycle, the now almost ideal amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXT} B and the output gain stage. C_{EXT} B and S2 act as a sample and hold to store the amplified input signal during the auto-zero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the auto-zero cycle the inputs are not only shorted together, but are also shorted to the negative input. This forces nulling with the common-mode voltage present. The same argument applies to power supply variations and accounts for the extremely good CMRR and PSRR specifications on the LTC1052.

The complete amplifier contains stabilizing elements, feed-forward for high frequency signals, and anti-aliasing circuitry, but the superior DC performance is completely described by this simple loop.

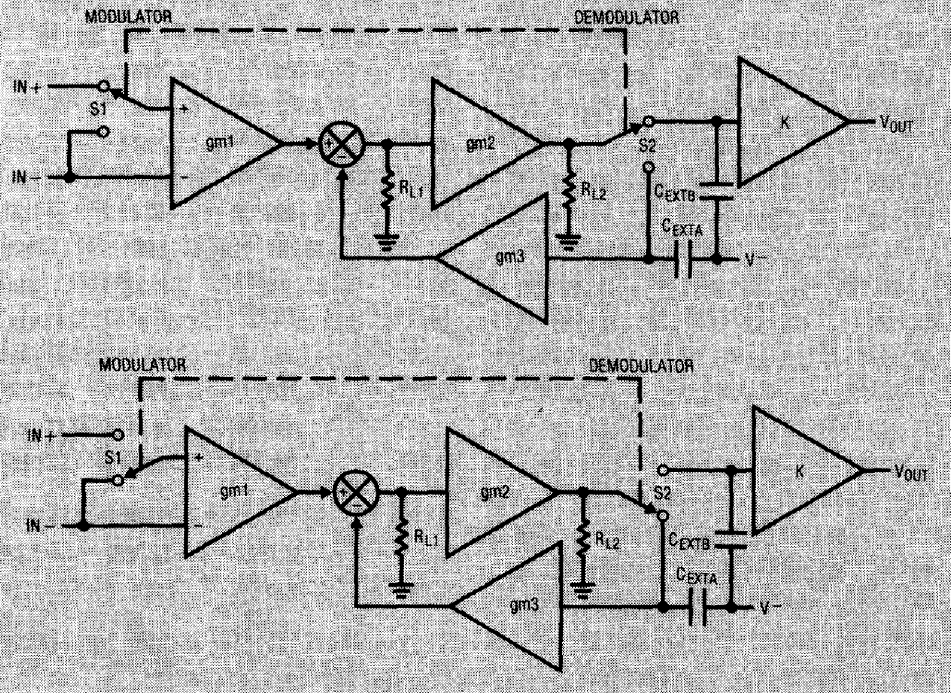

Figure B3. LTC1052 Conceptual Amplifier (Simplified)

References

Goldberg, E. A. ''Stabilization of Wideband Amplifiers for Zero and Gain'', RCA Review, June, 1950, page 298.

SP656 Data Sheet, Philbrick Researches, 1963.

Brokaw, A. P. ''Designing Sensitive Circuits? Don't Take Grounds for Granted'', EDN, October 5, 1975, page 44.

Morrison, Ralph, ''Grounding and Shielding Techniques in Instrumentation'', 2nd Edition, Wiley Interscience, 1977.

Ott, Henry W., ''Noise Reduction Techniques in Electronic Systems'', Wiley Interscience, 1976.

Hueckel, John H., ''Input Connection Practices for Differential Amplifiers'', Neff Inst. Corp., Duarte, California.

''Elimination of Noise in Low-Level Circuits'', Gould, Inc., Instrument Systems Division, Cleveland, Ohio.

Williams, J., ''Prevent Low Level Amplifier Problems'', Electronic Design, February 15, 1975, page 62.

Pascoe, G., ''The Choice of Solders for High-Gain Devices'', New Electronics (Great Britain), February 6, 1977.

Pascoe, G., ''The Thermo-E.M.F. of Tin-Lead Alloys'', Journal Phys. E: December, 1976.